2023

COMPUTER APPLICATION

Paper : BCAHC3066

(Digital Logic Fundamentals)

Full Marks : 60
Pass Marks : 24

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Choose the correct answer (any *five*) : 1×5=5

   (a) Register is a

   (i) combinational circuit

   (ii) sequential circuit

   (iii) Both *(i)* and *(ii)*

   (iv) combination of flip-flop

(b) The Boolean function $A+BC$ is a reduced form of

(i) $AB+BC$

(ii) $(A+B)(A+C)$

(iii) $A'B+AB'C$

(iv) $(A+C)B$

(c) How many gates would be required to implement the following Boolean expression after simplification?

$$XY+X(X+Z)+Y(X+Z)$$

(i) 1

(ii) 2

(iii) 4

(iv) 5

(d) Applying the distributive law to the expression $A(B+\bar{C}+D)$, we get

(i) $AB+AC+AD$

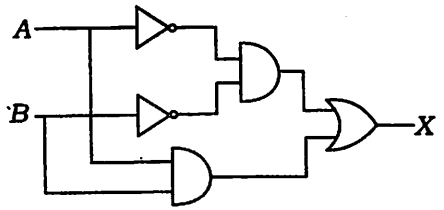
(ii) $ABCD$

(iii) $A+B+C+D$

(iv) $AB+A\bar{C}+AD$

(Continued)

(e) Which of the following logic expressions represents the logic diagram shown?



(i) $X=AB'+A'B$

(ii) $X=(AB)'+AB$

(iii) $X=(AB)'+A'B'$

(iv) $X=A'B'+AB$

(f) 3 bits full adder contains

(i) 3 combinational inputs

(ii) 4 combinational inputs

(iii) 6 combinational inputs

(iv) 8 combinational inputs

(g) Which condition is shown in J-K flip-flop as no changes next state from next state?

(i) $J=0,\ K=0$

(ii) $J=0,\ K=1$

(iii) $J=1,\ K=0$

(iv) $J=1,\ K=1$

(Turn Over)

(h) A register capable of incrementing and/ or decrementing its contents

(i) counter

(ii) decoder

(iii) multiplexer

(iv) demultiplexer

(i) How many *J-K* flip-flops are required to achieve a frequency division of 8?

(i) 1

(ii) 2

(iii) 3

(iv) 4

(j) A module 10-counter must have

(i) 10 flip-flops

(ii) 4 flip-flops

(iii) 2 flip-flops

(iv) synchronous clocking

(Continued)

2. Answer any *five* the following question : 2×5=10

(a) Design logic diagram and block diagram of the full adder using two half-adders.

(b) What is flip-flop?

(c) State the duality principle.

(d) Convert $(7CF)_{16} = (?)_2$.

(e) Convert $(1DA6)_{16}$ to decimal.

(f) Write the truth table of AND gate using three inputs.

(g) How do you overcome the limitations of propagation delay in ripple counters?

3. Answer any *six* of the following questions : 5×5=25

(a) Design a (4 : 1) multiplexer.

(b) Convert to the canonical forms

$$F(x, y, z) = \Sigma(1, 3, 7)$$

(c) Explain the applications of bidirectional shift registers.

(Turn Over)

(d) What is T flip-flop? Explain clocked J-K flip-flop with its logic diagram and truth table.

(e) What are universal logic gates? Realize NAND and NOR as universal logic gates.

(f) What is register? Explain the types of registers depending on input-output with its block diagram and logic diagram.

(g) Explain the concepts of minterm and maxterm expressions with examples.

(h) Construct a 4×16 decoder with two 3×8 decoders.

(i) Covert the expressions to sum-of-products terms :

(i) $(A+B)(B'+C)(A'+C)$

(ii) $(A'+C)(A'+B'+C')(A+B')$

4. Answer any *two* of the following questions : $10 \times 2 = 20$

(a) Explain 4-bit register with parallel load.

(b) Explain the concept of BCD counter with parallel load.

(Continued)

(c) Reduce the following expression by using Karnough map (K-map) technique :

$F(A, B, C, D) = \Sigma(0, 1, 2, 4, 5, 8, 9, 10, 11)$

(d) What are SOP and POS? Explain with example.

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