CRISP: A Flexible Integrated Development Platform for RFID Systems

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ABSTRACT

In this paper we present an introduction to Cognitive RFID Integrated System Platform (CRISP), a framework for development and implementation of RFID communication protocols. The framework enables advanced research in the area of RFID wireless communication protocols and algorithms by interfacing a large class of experimental medium access control (MAC) with custom physical layer (PHY) implementations. As such, CRISP provides a flexible, scalable, configurable and high performance RFID research tool. The low level protocol handling routines are written in VHDL and higher level functions are programmed in C and targeted to embedded Microblaze soft-core processor within the Xilinx Virtex 5 class of FPGAs. Furthermore, the online open-access repository from The University of Adelaide is available to document and share different architecture and designs with other researchers in the field.

Keywords: FPGA, RFID, Interrogator, RFID Reader, Passive RFID

1. INTRODUCTION

Radio Frequency Identification (RFID) is a form of enabling technology that enables machines to collect information through wireless sensors.[1] Warehouses will sense whether they become low on stock or, even perhaps, overstocked. Luggage will be routed automatically from airport to airport. Healthcare, libraries and many other institutions will be all influenced if not changed by RFID.[2] The benefits are potentially immense. RFID technologies are rapidly becoming ubiquitous for product identification as businesses seek to improve supply chain operations and respond to mandates from key customers.

The UHF readers cost upto several thousands dollars in price, depending on their functionality. Low functionality (dumb) readers are readers with limited computing power. They tend to be cheaper than intelligent readers, which typically have on-board computing power and can filter data, store information and execute commands. An intelligent reader, however, can communicate with tags using a variety of protocols, and operate at multiple frequencies[3] They may also have on-board computing power for filtering data and running applications and performing tag authentications.

RFID systems are demanding more data, faster logging, and higher interrogation rates, so they require a powerful system that can manage information from a variety of sources, store the data, and transmit it reliably and continuously for long periods of time to other readers or a host PC. The most common RFID readers in use today operate at Ultra High Frequency (UHF) and High Frequency (HF) Industrial, Scientific and Medical (ISM) bands. More and more wireless devices are being designed to utilize the ISM band. As the number of these wireless devices proliferates, so does the level of destructive noise in the spectrum that can hamper the effective use of RFID.[4]

To address the insatiable desire of the spectrum users for additional wireless bandwidth and burgeoning problem of spectrum scarcity, novel innovation in RFID reader technology and communication protocols are paramount. However, commercial RFID readers are like a black box. Low-level communication layer parameters and protocol specifics are hardwired, making it difficult, if not impossible for researchers to experiment and implement new functionality at those levels.

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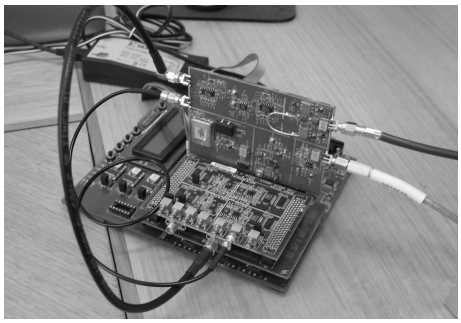

Figure 1. CRISP is designed to be reprogramable and makes maximum use of COTS components.

The purpose of this work is to provide the details of a portable, powerful and flexible software-defined RFID development platform. The system achieves these objectives by exposing low-level user-defined parameters and functions at each communication layer, thus providing an invaluable research tool in the field of RFID.

2. CRISP ARCHITECTURE

CRISP is build mostly upon standard commercial of the shelf components (COTS). It consists of four key components: mainboard hardware, board support packages, firmware and an Internet based open access document repository website. These key attributes provide a powerful, scalable and reconfigurable integrated system development platform for research in RFID era. Figure 1 shows the CRIPS main board along with its analog front-end boards.

Figure 2 shows the partitioning of the CRISP architecture. The RF module consists of an oscillator, waveform generator, RF power control, modulation, demodulation, signal conditioning and amplification. The digital modem part takes care of preamble detection, sequence estimation, coding and decoding of the signal and other low level signal processing tasks. The DSP firmware has the task of controlling and monitoring the RF module and providing a set of API functions through its interface to the application processor.

2.1. Mainboard Hardware

The balance between the computational needs of a smart RFID system and the flexibility and programmability needed for such application, CRISP uses the Xilinx Vertix 5 FPGA as its primary communication processor. The Microblaze soft-core processor available from Xilinx provides a complete embedded platform environment for MAC and PHY layer design. An experimental multi-board communication bus, based on opencore Wishbone[5]* is under development at The University of Adelaide that would provide high speed board to board connections, making the CRISP platform even more scalable and extendable.

Commercial RFID hardware is proprietary, as such low-level access to communication parameters are not available to the end users. CRISP is build to provide essential open source development platform for research at MAC and PHY levels. However the flexibility offered by the platform does not compromise its operational performance. The performance objective is achieved through the use of a state-of-the-art FPGA processor that is capable of handling multiple Microblaze cores along with hundreds of multiplier and accumulator cores (MAC) to perform high speed low level signal processing tasks in parallel. The main board is equipped with daughtercard slots that can be used to connect modular analog front-end boards (radio boards). Multiple analog boards can be plugged onto the system concurrently, building an RFID system that can operate at different frequency bands simultaneously. The availability of these multiple analog fornt-end boards provides a test-bed for development of novel communication links based on multi-input multi-output (MIMO) system. The presence of multi channel DAC board allows the monitoring of internal digital signals, using an oscilloscope.

The following provides some reasoning for choosing an FPGA to performing different functionality in the CRISP hardware:

*The Wishbone bus is a common interface between IP cores in an FPGA device.

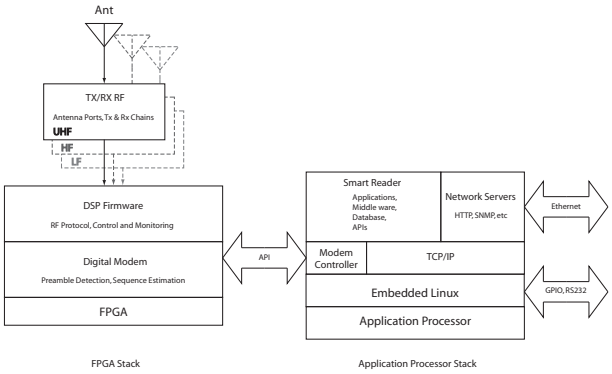

Figure 2. A simplified block diagram of CRISP architecture.[?]

- **FPGAs are flexible**
  Like many micro-controllers, FPGA can be programmed in the field in only a fraction of a second. Design revision can be implemented quickly and painlessly. Hardware can also be reduced by taking advantage of reconfigure-abilities.

- **Highly integrated**
  The programmable logic devices within an FPGA can absorb much of the interface, ie. glue logic, associated with microprocessors. The tight integration can make the product smaller, lighter, cheaper that can run at lower power levels.

- **Competitively priced**
  FPGAs are generic products that are customized at the point of use. They are relatively low price because of the high production volumes. They do not suffer the fabrication delays associated with ASIC development.

- **Fast turn around**
  The FPGAs' flexibility eliminates the long design cycle compared with ASICs. There are no delays for prototyping and sample productions. Design revision can be easily implemented in relatively short period of time. These devices are fully tested by the manufacturer, thus eliminating further test required by software development team.

2.2. Development software

The platform supports different levels of design architecture. At lowest level a design can be implemented in VHDL/VeriLog at RTL, behaviour or structural levels. The HDL code can also be generated automatically using system level Matlab modelling. Xilinx provides a set of library functions, known as DSP Tools, to facilitate such tasks. DSP Tools provides abstraction for building and debugging high performance DSP systems in Matlab using Simulinnk graphical interface. This tool set also provides hardware co-simulation that expedites the hardware in the loop simulation, which also provides clock accurate results.

For higher network levels, the C programming language is more appropriate as it provides faster and easier way to implements such functionality. The code can then be compiled to run on the Microblaze soft-core processor. A multiple number of such processors can be implemented in Virtex5, allowing the design to be broken into smaller chunks and run in parallel to achieve faster response.

For example consider a situation where there are multiple number of tags present in the reading range of a reader. These tags could arrive from different sources and might follow different standards. Keeping in mind that tags can respond with different coding and modulation schemes, a reader to understand the reply form a tag, would try to decode the response using a particular coding technique and if the result is not clear, is then tries to re-interrogate the tag with different coding method. The reader must also repeats the decoding process at least twice per reply it receives, once for In-phase (I) and next for Quadrature (Q) response. While a system with multiple processing cores can do all that in parallel and thus speed up the response quite considerably.

2.3. Daughter Boards

The FPGA main board is designed to be expandable, so it comes with peripheral card slots that could be used to connect a peripheral card to a large number of dedicated FPGA I/O pins. The slots are flexible enough to allow a large variety of existing and future peripheral designs. Currently only the RF (Radio) Module is being implemented by our group. This card can be easily replaced with one that best suits an end user application. The slots are well documented so the future development of custom peripheral cards can be undertaken by other researches.

The presense of multiple slots also allows development of Multiple-Input-Multiple-Output (MIMO) systems. As such the system not only can be used to develop advanced RFID concepts, but also be used in other active research areas such as development of sophisticated multimedia applications.

2.4. Open Access SVN

The University of Adelaide provides an open access repository to the public (that is currently under construction.) The CRISP repository is accessible through the Internet, and acts as a central archive for all the hardware and software designs. Any interested party can download the designs and clone this system and make contribution to the project, though the code contributions must be moderated by the project system administrator before being uploaded to the repository.

2.5. Application Development

Although there are numerus literature published in the field of RFID to tackle the current challenges, most of them are pure theory and some rely only on simulation. The reason being there is no open hardware research platform available to researchers in this field. CRISP was developed to address these issues.

CRISP is a unique platform that brings simulation and implementation one step closer. It is a platform to design, develop and test advanced RFID communication protocols in Physical (PHY) and Medium Access Control (MAC) layers.

Low-level signal processing functions are programmed in HDL code and implemented directly in hardware, while higher level PHY and MAC management routines are programmed in C and are targeted to Microblaze. The programmability of low level network layers and exposure of their operational parameters to an end user (researchers), allows them to develop various advanced custom networking protocols.

CRISPs main board is based on the Virtex5 FPGA from Xilinx. It provides significant processing resources in terms of CPU for general purpose processing as well as DSP core for application specific digital signal processing.

The Microblaze CPU core runs on an embedded version of Linux operating system, uClinux, and comes with a number of PC like functionalities built in. Linux being a mature operating system, allows the running of many applications that facilitate the operation of an RFID system. For instance it can run its own SQL database that applications can run queries against. Companies and third-party software developers can also write applications to run on the Linux operating system with minimum effort.

In addition, Linux has built-in support for standard networking protocols including DHCP, UDP/IP over Ethernet, 820.11x (Wi-Fi), HTTP and SNMP. Also, CRISP being a network based device allows us to upgrade and/or control the device remotely via the Ethernet.

3. CONCLUSION

In this paper we introduced Cognitive RFID Integrated System Platform (CRISP), a novel RFID research platform developed at the Auto-ID Lab of the University of Adelaide. This platform can be used by researchers and RFID developers to prototype various RFID communication protocols and algorithms. The system is based upon a Vertix5 processor, a state-of-the-art FPGA form Xilinx. The main board is equipped with expansion header pins that can be used to connect daughterboard. A daughter board can be an ADC/DAC board or an analogue front-end (radio) board, or some other custom made board for different purpose, such a display driver so that the device can be connected directly to a computer monitor to probe the internal state of the system.

The CRISP project also employs an Internet based code repository storage that can be used by reachers to download the latest design and/or update their improvement to the current system.

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